What is claimed is:

1. A deinterleaving apparatus for a digital communication system, comprising:

a row counter for increasing a row counting value based on input data;

a column counter for increasing a column counting value in every row period set in the row counter;

plural synchronous counters corresponding to the row period, and for increasing a synchronous counting value in every column period set in the column counter;

an offset memory for storing offset values set in correspondence to interleaving delay depths of the input data for each channel; and

a deinterleaver memory for storing the input data at a write address generated based on the offset values, wherein the input data stored in the deinterleaver memory is read at a read address generated based on the synchronous counting value.

2. The deinterleaving apparatus as claimed in claim 1, wherein the plural synchronous counters each have a different synchronous period from each other in correspondence to the row counting value.

3. The deinterleaving apparatus as claimed in claim 1, wherein a column period set in the column counter corresponds to a synchronous signal of the digital communication system.

4. The deinterleaving apparatus as claimed in claim 1, wherein the input data includes valid and invalid data depending upon interleaving delay depths for each channel, and the valid data is read at the read address generated based on the synchronous counting value.

5. The deinterleaving apparatus as claimed in claim 1, wherein the read and write addresses are generated in combination of the row counting value, column counting value, and synchronous counting value.

6. The deinterleaving apparatus as claimed in claim 1, wherein the write address is generated based on the column counting value to which the offset value is added and the synchronous counting value.

7. The deinterleaving apparatus as claimed in claim 1, further comprising plural multiplexers for selectively switching, so as to output a signal for writing and reading with respect to the deinterleaver memory.

8. A deinterleaving method for a digital communication system, comprising steps of:

increasing a row counting value of a row counter based on input data;

increasing a column counting value of a column counter every row period set in the row counter;

increasing synchronous counting values of plural synchronous counters every column period set in the column counter;

storing in a deinterleaver memory the input data at a write address generated based on offset values set in correspondence to interleaving delay depths of the input data for each channel; and

reading the input data stored in the deinterleaver memory at a read address generated based on the synchronous counting values.

9. The deinterleaving method as claimed in claim 8, wherein the plural synchronous counters each have a different synchronous period from each other in correspondence to the row counting value.

10. The deinterleaving method as claimed in claim 8, wherein a column period set in the column counter corresponds to a synchronous signal of the digital communication system.

11. The deinterleaving method as claimed in claim 8, wherein the input data includes valid and invalid data depending upon interleaving delay depths for each channel, and, in the data-reading step, the valid data is read for an output at the read address generated based on the synchronous counting value.

12. The deinterleaving method as claimed in claim 8, wherein the read and write addresses are generated in combination of the row counting value, column counting value, and synchronous counting value.

13. The deinterleaving method as claimed in claim 8, wherein the write address is generated based on the column counting value to which the offset value is added and the synchronous counting value.

14. The deinterleaving method as claimed in claim 8, wherein each step further includes a step for selectively outputting a signal with respect to a predetermined input signal.